REMARKS

In response to the office action of 11/03/2005, the applicant has provided the following remarks:

Request for Continued Examination

Applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1-22 are rejected under 35 USC 102e as being anticipated by Jeansonne et al. (US2004/0205280)

Claims 1-22 are cancelled.

New Claims 23-42

New claims 23-42 have been added in an effort to accurately describe and detail the present invention, and to further distinguish its uniqueness and novelty over the teachings of Jeansonne et al. No new matter is entered by the new claims. Further comments about the patentability of the new claims with respect to the teachings of Jeansonne et al. are provided below.

Introduction of Independent Claims 23 and 33

Applicant has introduced a new independent claim 23 to distinctly describe the present invention and differentiate its novelty over references provided by the Examiner. Applicant would like to particularly point out that claim 1 makes reference to "a plurality of activation circuits, each activation circuit(emphasis added) corresponding to a bridge chip and being for disabling the corresponding bridge chip until a predetermined protocol initialization signal sent by the host system is received by the activation circuit". In this way, prior to any predetermined protocol initialization signal being sent, all bridge chips must be initially disabled. This feature differs from the invention of Jeansonne et al., as Jeansonne shows that enabling/disabling of the bridge chips is performed by a control signal that is inputted

to one bridge chip while being inverted then inputted to another (Jeansonne, Fig 4 elements 78,80). The inversion of the control signal by Jeansonne will in fact ensure that at least one of the bridge chips will be initially enabled. This contrasts the present invention in which all the bridge chips are initially disabled until reception of a protocol initialization signal. Furthermore, Jeansonne shows in Fig, 9 that the control signal (which was previously interpreted by the Examiner as a "predetermined protocol initialization signal") is sent from the component (device) in order to activate the desired bridge chip. This contrasts new claim 23 of the present invention as the "predetermined protocol initialization signal sent by the host system" states that the host system sends the signal.

In addition, newly introduced Claim 23 describes the present invention as a bridge for coupling multiple host bus interfaces to a single device bus interface. This is further illustrated in Fig. 4 of the present invention, showing multiple host bus interfaces (elements 30,35) coupled to a bridge (element 120), which in turn is further coupled to a single device bus interface (element 40). Conversely, it is clear from at least Fig. 2 of Jeansonne et al. that a bridge (element 40) is presented for connecting multiple device bus interfaces (elements 62,64) to a single host bus interface (element 46).

For at least the above reasons applicant asserts that newly added claim 23 should be found allowable with respect to the teachings of Jeansonne et al. Similar comments also apply to independent method claim 33. Consideration of independent claims 23 and 33 is respectfully requested. As claims 24-32 and 33-42 are dependent on claim 23 and claim 33 respectively, if claims 23 and 33 are found allowable, so too should claims 24-32 and 33-42.

Introduction of Dependant Claims 24,25 and 34,35

These claims highlight the function of the activation circuits in the present invention to disable all of the bridge chips upon a hardware reset or a power on such that none of the bridge chips control the device bus interface. Jeansonne et al. do not teach disabling a bridge chip upon a hardware reset or power on. Furthermore, from at

least Fig. 4 of Jeansonne, it is clear that at least one of the bridge chips will control the device bus interface due to inversion of the control signal (element 80).

Introduction of Dependant Claim 26 and 36

These claims highlight the function of a bridge chip described in the present invention to maintain control of the device bus interface until a hardware reset occurs. This concept is not taught by Jeansonne. From at least Fig. 4 of Jeansonne et al. it is evident that should a device be coupled to the endpoint with the bridge controlling the device bus interface, a simple toggling of the control signal will disable the bridge chip in operation and cause it to lose control of the device bus interface. This example illustrates that the invention of Jeansonne et al. does not necessarily maintain control of the device (and hence device bus interface) once a bridge chip is enabled. That is, according to the teachings of Jeansonne et al., insertion of other devices may cause a currently controlling bridge chip to loose control.

Sincerely yours,

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